Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	271	345/537.ccls.	US-PGPUB; USPAT	OR	OFF	2005/03/10 08:39
S2	115	345/539.ccls.	US-PGPUB; USPAT	OR	OFF	2005/03/10 12:39
S3	489	345/536.ccls.	US-PGPUB; USPAT	OR	OFF	2005/03/09 16:49
S4	237	345/530.ccls.	US-PGPUB; USPAT	OR	OFF	2005/03/09 15:17
S5	432	345/545.ccls.	US-PGPUB; USPAT	OR	OFF	2005/03/09 15:18
S6	70	345/539.ccls. and controller	US-PGPUB; USPAT	OR	OFF	2005/03/09 15:53
S7	44	345/539.ccls. and controller and frame adj buffer	US-PGPUB; USPAT	OR	OFF	2005/03/09 15:19
S8	22	345/539.ccls. and controller and frame adj buffer and refresh	US-PGPUB; USPAT	OR	OFF	2005/03/09 15:19
S9	12	345/539.ccls. and controller and frame adj buffer and refresh and chip	US-PGPUB; USPAT	OR	OFF	2005/03/09 15:19
S10	11	345/539.ccls. and controller and frame adj buffer and refresh and chip and register	US-PGPUB; USPAT	OR	OFF	2005/03/09 15:19
S13	6	345/539.ccls. and controller and frame adj buffer and refresh and chip and register and clock adj signal	US-PGPUB; USPAT	OR	OFF	2005/03/09 15:45
S14	35	345/539.ccls. and chip	US-PGPUB; USPAT	OR	OFF	2005/03/09 15:53
S15	12	345/539.ccls. and chip and external and internal	US-PGPUB; USPAT	OR	OFF	2005/03/09 15:58
S17	2	345/539.ccls. and chip and external adj memory and internal adj memory	US-PGPUB; USPAT	OR	OFF	2005/03/09 16:02
S20	167	double adj buffer$3 and chip and external adj memory and internal adj memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:02
S21	97	double adj buffer$3 and chip and external adj memory and internal adj memory and frame adj buffer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:02

S22	95	double adj buffer$3 and chip and external adj memory and internal adj memory and frame adj buffer and controller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:03
S23	77	double adj buffer$3 and chip and external adj memory and internal adj memory and frame adj buffer and controller and refresh	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:03
S24	77	double adj buffer$3 and chip and external adj memory and internal adj memory and frame adj buffer and controller and refresh and register	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:07
S25	4	double adj buffer$3 and chip and external adj memory and internal adj memory and frame adj buffer and controller and refresh and register and clock adj signal	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:03
S28	77	double adj buffer$3 and chip and external adj memory and internal adj memory and frame adj buffer and controller and refresh and register and clock	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:47
S42	564	double adj buffer$3 and portable	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:50
S43	7	double adj buffer$3 and portable adj power	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:53
S45	32	portable adj power and external adj memory and internal adj memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:56

S48	30	portable adj power and external adj memory and internal adj memory and display	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:54
S49	28	portable adj power and external adj memory and internal adj memory and display and graphics	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:54
S50	27	portable adj power and external adj memory and internal adj memory and display and graphics and chip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:54
S51	27	portable adj power and external adj memory and internal adj memory and display and graphics and chip and refresh	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:54
S52	27	portable adj power and external adj memory and internal adj memory and display and graphics and chip and refresh and clock	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 16:55
S54	8	345/539.ccls. and recent	US-PGPUB; USPAT	OR	OFF	2005/03/10 12:45
S55	96	345/539.ccls. and new	US-PGPUB; USPAT	OR	OFF	2005/03/10 12:46
S56	66	345/539.ccls. and new same buffer	US-PGPUB; USPAT	OR	OFF	2005/03/10 12:46
S57	22	345/539.ccls. and new same buffer and chip	US-PGPUB; USPAT	OR	OFF	2005/03/10 12:47
S58	9	345/539.ccls. and new same buffer and chip and external	US-PGPUB; USPAT	OR	OFF	2005/03/10 15:59
S59	23	345/539.ccls. and clock adj signal	US-PGPUB; USPAT	OR	OFF	2005/03/10 16:24
S62	9	345/539.ccls. and clock adj signal same write	US-PGPUB; USPAT	OR	OFF	2005/03/10 16:03
S63	9	345/539.ccls. and clock adj signal same write and read and write	US-PGPUB; USPAT	OR	OFF	2005/03/10 16:15

S64	290	double adj buffer$3 and clock adj signal same write and read and write	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/10 16:16
S65	60	double adj buffer$3 and clock adj signal same write and read and write and frame adj buffer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/10 16:16
S66	56	double adj buffer$3 and clock adj signal same write and read and write and frame adj buffer and controller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/10 16:16
S67	45	double adj buffer$3 and clock adj signal same write and read and write and frame adj buffer and controller and external	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/10 16:40
S68	11	double adj buffer$3 and clock adj signal same write and read and write and frame adj buffer and controller and external adj memory and internal adj memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/10 16:17
S69	11	double adj buffer$3 and clock adj signal same write and read and write and frame adj buffer and external adj memory and internal adj memory	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/10 16:18
S70	11	double adj buffer$3 and clock adj signal same write and read and write and frame adj buffer and external adj memory and internal adj memory and chip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/10 16:18
S71	11	double adj buffer$3 and clock adj signal same write and read and write and frame adj buffer and external adj memory and internal adj memory and chip and register	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/10 16:19
S72	9	345/539.ccls. and clock adj signal and double adj buffer$3	US-PGPUB; USPAT	OR	OFF	2005/03/10 16:29
S74	24	345/539.ccls. and clock and double adj buffer$3	US-PGPUB; USPAT	OR	OFF	2005/03/10 16:30

S75	22	345/539.ccls. and clock and double adj buffer$3 and read and write	US-PGPUB; USPAT	OR	OFF	2005/03/10 16:32
S76	13	345/539.ccls. and clock same write and double adj buffer$3 and read	US-PGPUB; USPAT	OR	OFF	2005/03/10 16:30
S77	56	double adj buffer$3 and clock adj signal same write and read and write and frame adj buffer and controller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/10 16:47
S79	33	double adj buffer$3 and clock adj signal same write same read and frame adj buffer and controller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/10 16:47